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online: EPODOC,WPI,JAPIO

(54) Abstract Title
Barrier layer for a semiconductor device

(57) A method for forming a barrier layer for a semiconductor device comprises the steps of first providing a semiconductor substrate 30 that has a conductive layer 31 already formed thereon. Then, a dielectric layer 32 such as an organic low-k dielectric layer is deposited over the conductive layer 31 and the semiconductor substrate 30. Next, an opening 33 is formed in the dielectric layer 32 exposing the conductive layer 31. Thereafter, a first barrier 34 layer is deposited into the opening 33 and the surrounding area. The first barrier layer 34 can be a silicon-containing layer or a doped silicon (doped-Si) layer formed by a plasma-enhanced chemical vapor deposition (PECVD) method, a low-pressure chemical vapor deposition (LPCVD) method, an electron beam evaporation method or a sputtering method. Finally, a second barrier layer 35 is formed over the first barrier layer 34, e.g. by CVD. The second barrier layer 35 can be a titanium/titanium nitride (Ti/TiN) layer, a tungsten nitride (WN) layer, a tantalum (Ta) layer or a tantalum nitride (TaN) layer. The opening is then filled with tungsten, copper or aluminium to form a via 36. The method can be applied to a damascene process.

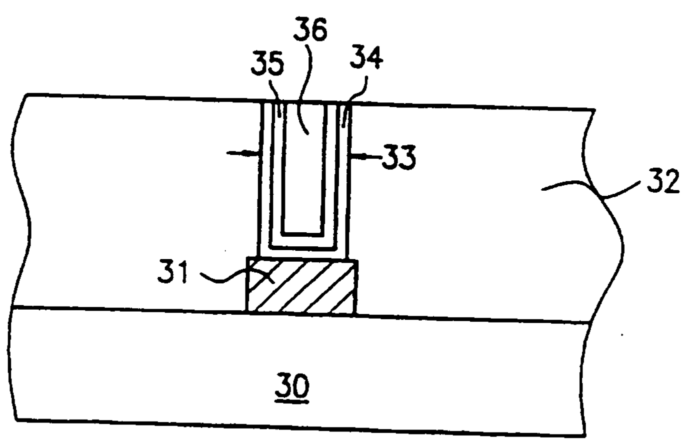

FIG. 3D

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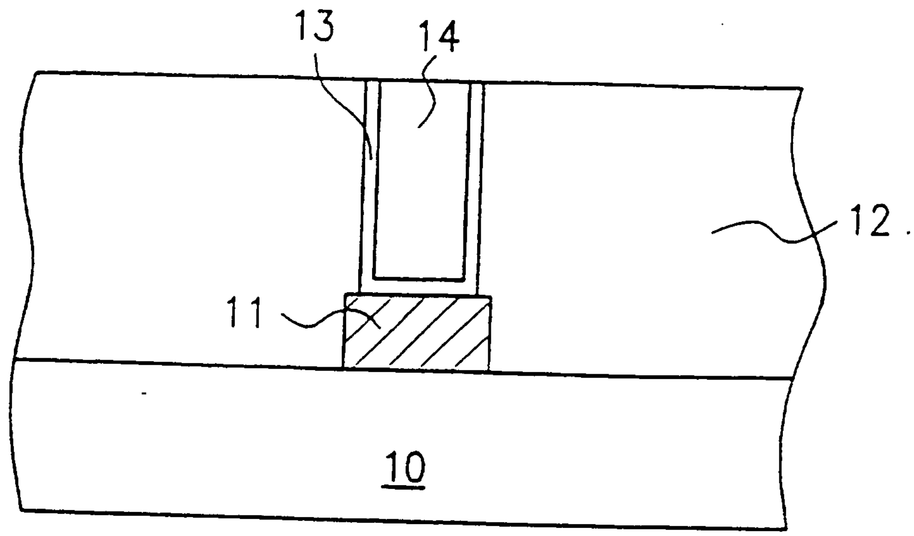

FIG. 1 (PRIOR ART)

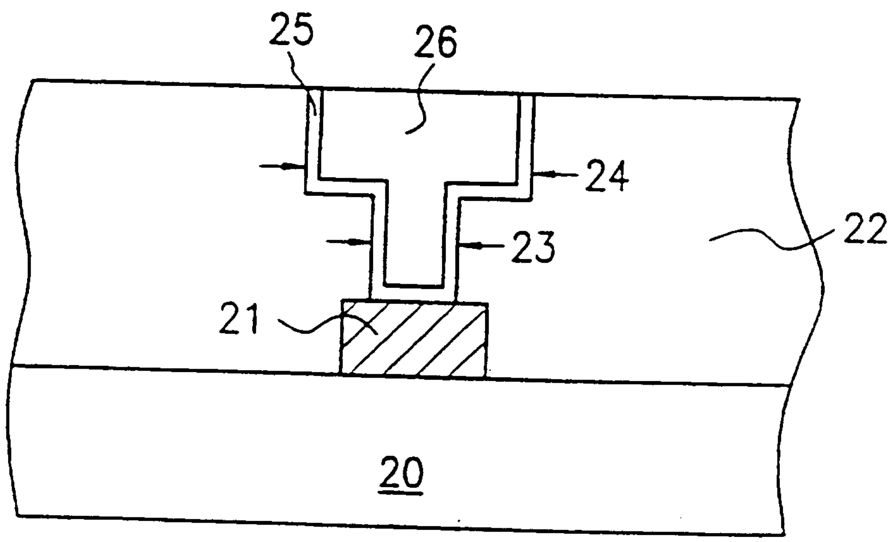

FIG. 2 (PRIOR ART)

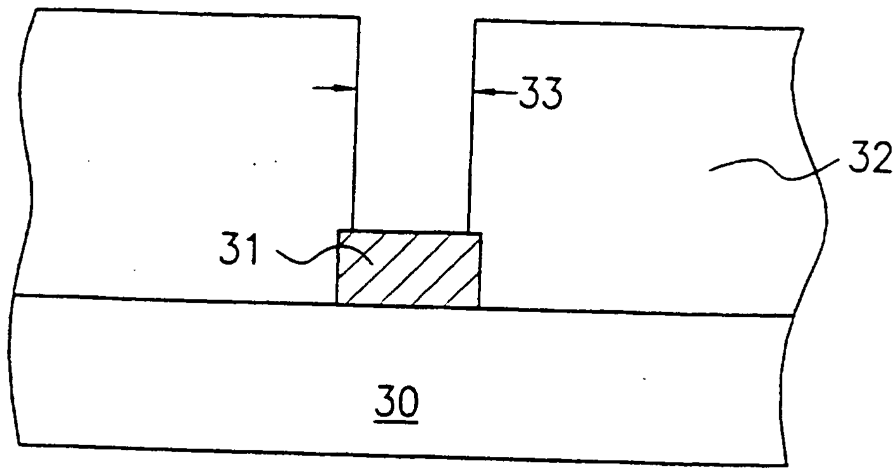

FIG. 3A

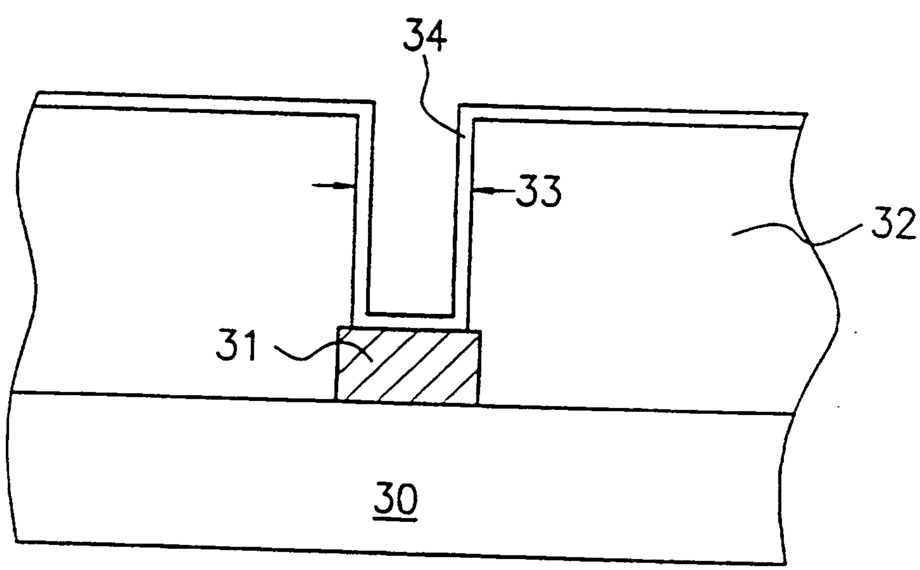

FIG. 3B

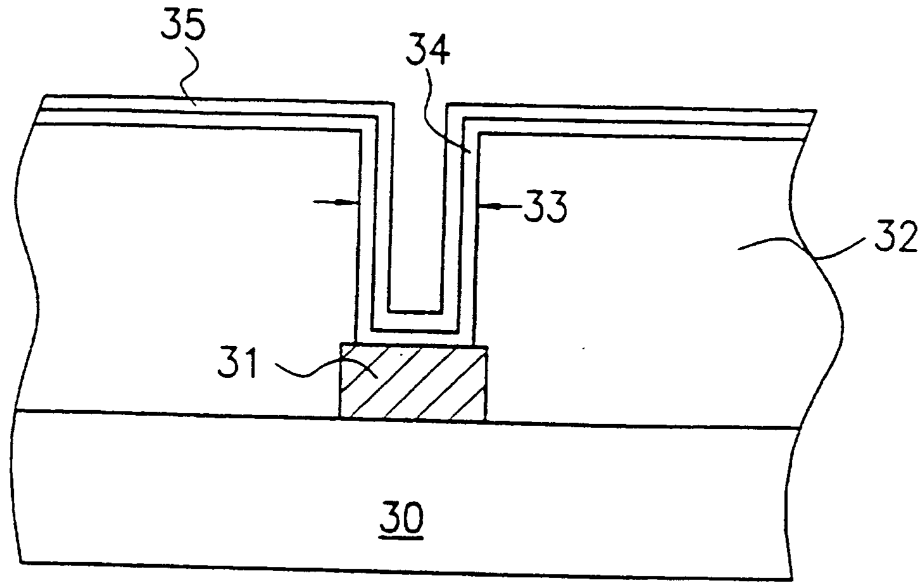

FIG. 3C

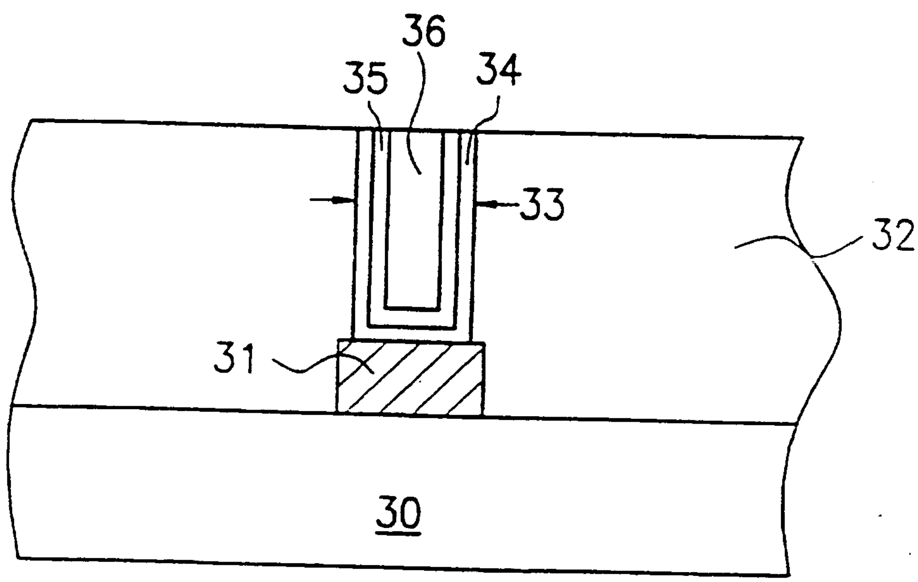

FIG. 3D

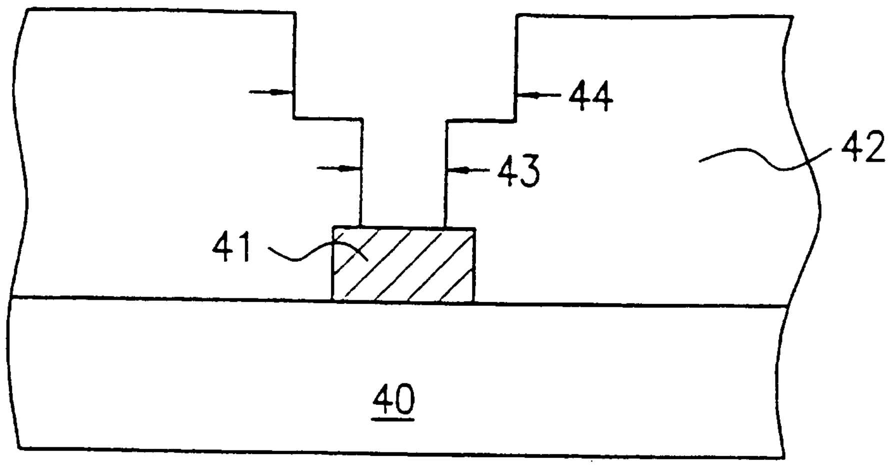

FIG. 4A

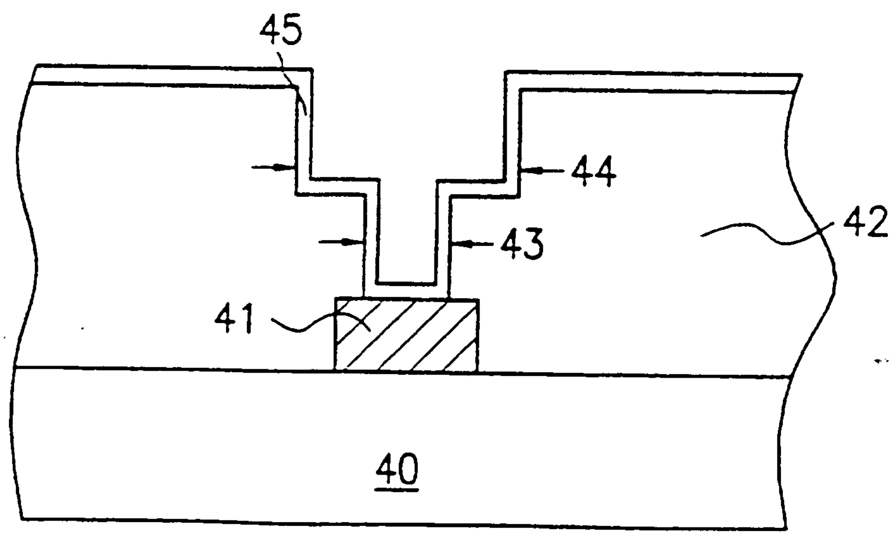

FIG. 4B

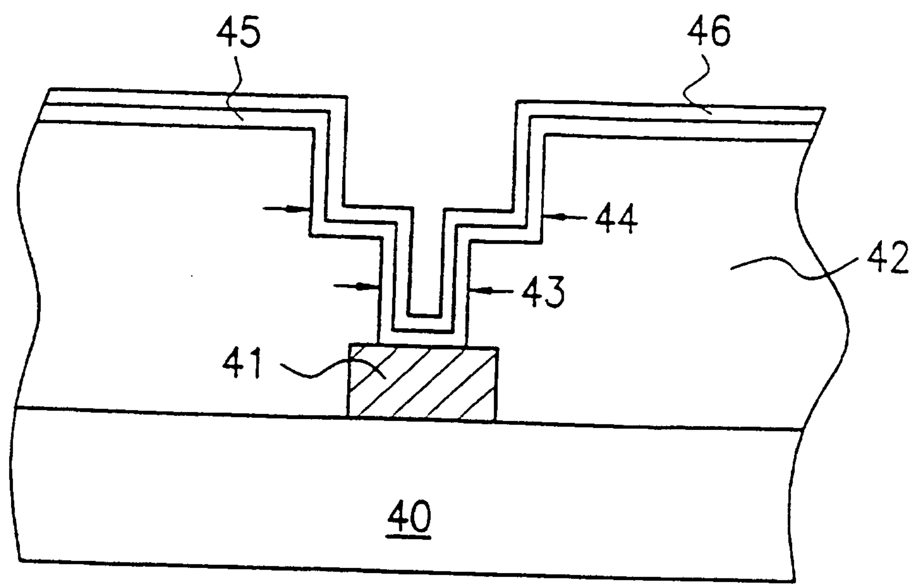

FIG. 4C

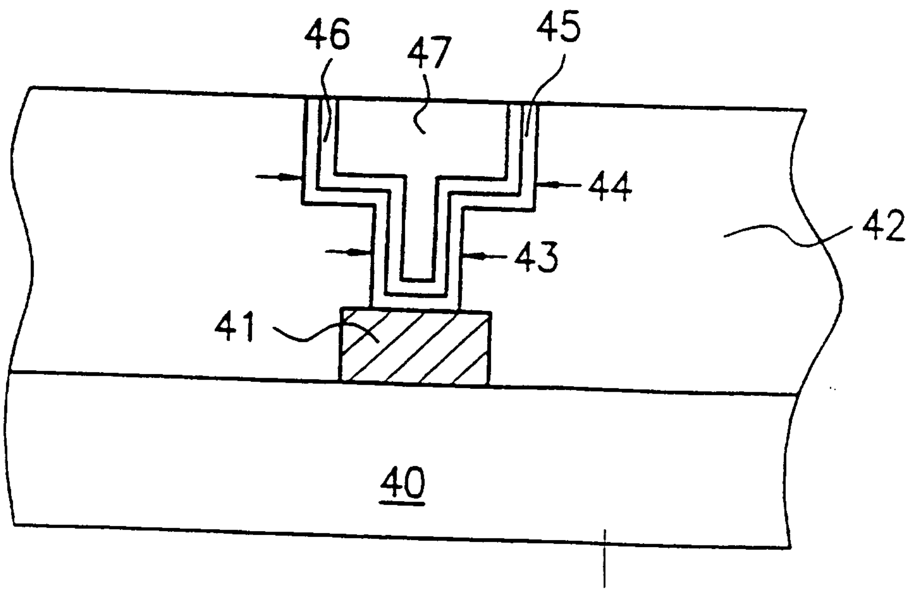

FIG. 4D

BARRIER LAYER AND FABRICATING METHOD OF THE SAME

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a barrier layer and method of fabrication the barrier layer. More particularly, the present invention relates to a barrier layer and method of fabrication the barrier layer that can enhance the adhesion of a via with low-k dielectric sidewalls.

Description of Related Art

In general, as the level of integration of integrated circuits increases, the number of metal interconnects necessary for interconnecting devices increases correspondingly. This is especially true in the fabrication of deep sub-micron VLSI circuits. One important and highly desirable property of metallic interconnects is a good electrical conductivity even when the contact area is very small. At present, the most common material for forming metallic interconnects is aluminum. However, copper has a lower resistance and a higher melting point. Therefore, as the level of integration continues to increase, copper has the potential to replace aluminum as a material for forming interconnects in the generation to come despite the many foreseeable problems that still exist.

Fig. 1 is a cross sectional diagram showing a conventional barrier layer structure. As shown in Fig. 1. the barrier layer structure is formed by first providing a semiconductor substrate 10, wherein a conductive layer 11 such as a metallic line

structure has already been formed above the substrate 10. Then, a dielectric layer 12 is formed over the conductive layer 11 and the substrate 10. The dielectric layer 12 can be formed using a low-k dielectric material. Next, a via 14 is formed in the dielectric layer 12, and then a highly conductive material such as tungsten, copper or aluminum is deposited into the via 14. In general, a barrier layer is also formed between the via 14 and the conductive layer and between the via 14 and the dielectric layer 12. The reason for forming the barrier layer 13 is to increase adhesion of conductive material onto the sides of the via 14 as well as to prevent the diffusion of conductive material into the dielectric layer. Nowadays, the most commonly used barrier layer materials include titanium/titanium nitride (Ti/TiN), tungsten nitride (WN), tantalum (Ta) and tantalum nitride (TaN).

Fig. 2 is a cross-sectional view showing a conventional barrier layer structure formed by a damascene process. As shown in Fig. 2, the barrier layer structure is formed by first providing a semiconductor substrate 20 having conductive layer 21 formed thereon. The conductive layer can be a first metallic line structure, for example. Next, a dielectric layer 22 is formed over the conductive layer 21 and substrate 20. The dielectric later 22 can be formed using a low-k dielectric material. Thereafter, a second opening 24 and a first opening 23 are sequentially formed in the dielectric layer 22. Subsequently, a barrier layer 25 is formed over the first opening 23 and the second opening 24. In general, the most common used barrier layer materials include titanium/titanium nitride (Ti/TiN), tungsten nitride (WN), tantalum (Ta) and tantalum nitride (TaN). The reason for having a barrier layer 13 is to increase the adhesive strength of subsequently deposited conductive material as well as to prevent the diffusion of conductive material to the dielectric layer. In the subsequent step, a

conductive layer 26 is deposited into the openings 23 and 24 and over the dielectric layer 22. The conductive layer 26 can be formed using a material that has good electrical conductivity, for example, tungsten, copper or aluminum. Finally, the conductive layer 26 is planarized using a chemical-mechanical polishing (CMP) operation to complete the damascene fabricating process. The advantage of using a damascene process includes its capacity for forming both a via and a second metallic line structure in the same processing operation. For example, a via structure is formed in the first opening 23 and a second metallic line structure is formed in the second opening 24.

The aforementioned methods of fabricating a barrier layer do have defects. First, if the material used for filling the via is copper (future trend), since cross-diffusion between copper and dielectric material is very strong, a barrier formed using conventional material and method cannot prevent diffusion. Organic low-k dielectric material is often used as a dielectric layer but the organic low-k dielectric material has poor adhesion with a conventional barrier layer material. This is because a low-k dielectric material has a high moisture absorption capacity; this is especially true for an organic low-k dielectric material. Therefore, a layer of moisture will be retained on the surface layer of the dielectric material. Hence, the dielectric layer can provide only poor adhesion with the subsequently deposited barrier layer and conductive layer.

In light of the foregoing, there is a need to provide a method of fabrication a barrier layer.

SUMMARY OF THE INVENTION

Accordingly, the present invention is to provide a barrier layer and method of fabricating the barrier layer that can increase the adhesion between a low-k dielectric layer and a barrier layer as well as to enhance the capacity of a barrier layer to prevent the diffusion of conductive material. In addition, the barrier layer is able to protect the surface of the low-k dielectric layer and minimize the effect of having a moisture-absorbing surface.

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a barrier layer structure. The barrier layer structure comprises a semiconductor substrate with a conductive layer formed on it and a dielectric layer formed over the conductive layer and the semiconductor substrate. The dielectric layer has an opening that exposes the conductive layer and can be, for example, an organic, low-k dielectric layer. There is also a first barrier layer deposited in the opening in the dielectric layer and its peripheral areas; this first barrier layer can be a layer containing silicon or a doped silicon (doped-Si) layer. A second barrier layer is formed above the first barrier layer and can be a titanium/titanium nitride (Ti/TiN) layer, a tungsten nitride (WN) layer, a tantalum (Ta) layer or a tantalum nitride (TaN) layer.

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of fabricating a barrier layer. First, a semiconductor substrate that has a conductive layer formed thereon is provided. Then, a dielectric layer such as an organic low-k dielectric layer is deposited over the conductive layer and the semiconductor substrate. Next, an opening is formed in the dielectric layer to expose the conductive layer.

Thereafter, a first barrier layer is deposited into the opening and the surrounding area. The first barrier layer can be a silicon-containing layer or a doped silicon (doped-Si) layer formed by a plasma-enhanced chemical vapor deposition (PECVD) method, a low-pressure chemical vapor deposition (LPCVD) method, an electron beam evaporation method or a sputtering method. Finally, a second barrier layer is formed over the first barrier layer. The second barrier layer can be a titanium/titanium nitride (Ti/TiN) layer, a tungsten nitride (WN) layer, a tantalum (Ta) layer or a tantalum nitride (TaN) layer.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Fig. 1 is a cross sectional diagram showing a conventional barrier layer structure;

Fig. 2 is a cross-sectional view showing a conventional barrier layer structure formed by a damascene process;

Fig. 3A through 3D are cross-sectional views showing the progression of manufacturing steps for forming a barrier layer over the surface of a via according to a first preferred embodiment of this invention; and

Fig. 4A through 4D are cross-sectional views showing the progression of

manufacturing steps for forming a barrier layer using a damascene process according to a second preferred embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

Figs 3A through 3D are cross-sectional views showing the progression of manufacturing steps for forming a barrier layer over the surface of a via according to a first preferred embodiment of this invention.

First, in Fig. 3A, a semiconductor substrate 30 having a conductive layer 31 formed thereon is provided. The conductive layer 31, for example, can be the source/drain region of a transistor or part of a metallic line structure. Next, a dielectric layer 32 is formed over the conductive layer 31 and the semiconductor substrate 30. The dielectric layer 32, can be, for example, an organic low-k dielectric layer or an oxide layer. Subsequently, the dielectric layer 32 is patterned to form an opening 33 exposing the conductive layer 31.

Next, as shown in Fig. 3B, the exposed semiconductor substrate 30 and the exposed dielectric layer 32 is cleaned using a dry or wet cleaning method. Thereafter, a plasma treatment is conducted to clean the exposed semiconductor substrate 30 and the exposed dielectric layer 32. The plasma treatment can be carried out using a plasma containing argon (Ar), hydrogen (H_2) or argon/hydrogen. Subsequently, a thin first barrier layer 34 is formed over the opening 33 and surrounding areas. The first

barrier layer 34 preferably having a thickness below 300 Å is a doped silicon layer (doped-Si) or a silicon-doped layer. The first barrier layer 34 can be formed by using a plasma-enhanced chemical vapor deposition (PECVD) method, a low-pressure chemical vapor deposition (LPCVD) method, an electron beam evaporation method or a sputtering method. The first barrier layer 34 is able to increase its adhesion with an organic low-k dielectric layer and lower moisture absorption of the organic dielectric layer.

Next, as shown in Fig. 3C, a second barrier layer 35 is formed over the first barrier layer 34. The second barrier layer 35, for example, can be a titanium/titanium nitride (Ti/TiN) composite layer, a tungsten nitride (WN) layer, a tantalum (Ta) layer or a tantalum nitride (TaN) layer, and is formed using a chemical vapor deposition method.

Finally, as shown in Fig. 3D, conductive material such as tungsten, copper or aluminum is deposited over the dielectric layer 32 and fills the opening 33. Then, the conductive layer is polished to expose the dielectric layer 32 using a chemical-mechanical polishing method. Hence, a via structure 36 is formed.

Figs. 4A through 4D are cross-sectional views showing the progression of manufacturing steps for forming a barrier layer using a damascene process according to a second preferred embodiment of this invention.

First, in Fig. 4A, a semiconductor substrate 40 having a conductive layer 41 formed thereon is provided. The conductive layer 41 can be, for example, the source/drain region of a transistor or part of a metallic line structure. Next, a dielectric layer 42 is formed over the conductive layer 41 and the semiconductor substrate 40. The dielectric layer 42 can be, for example, an organic low-k dielectric layer or an oxide layer. Subsequently, the dielectric layer 42 is patterned to form a first opening 44,

where depth of the first opening 44 is smaller than the thickness of the dielectric layer 42. After that, the dielectric layer 42 is further etched to form a second opening 43 that exposes the conductive layer 41 below the first opening 44, where the second opening 43 has a width smaller than the first opening 44.

Next, as shown in Fig. 4B, the exposed semiconductor substrate 40 and the exposed dielectric layer 42 are cleaned using a dry or wet cleaning method. Thereafter, a plasma treatment is further conducted to clean the exposed semiconductor substrate 42 and the exposed dielectric layer 42. The plasma treatment can be carrier out using a plasma containing argon (Ar), hydrogen (H_2) or argon/hydrogen. Subsequently, a first barrier layer 45 is formed over the first opening 44k the second opening 43 and surrounding areas. The first barrier layer 45, preferably having a thickness below 300Å, is a doped silicon layer (doped-Si) or a silicon-doped layer. The first barrier layer 34 can be formed by using a plasma-enhanced chemical vapor deposition (PECVD) method, a low-pressure chemical vapor deposition (KPCVD) method, an electron beam evaporation method or a sputtering method. The first barrier layer 45 is able to increase its adhesion with an organic low-k dielectric layer and lower moisture absorption of the organic dielectric layer.

Next, as shown in Fig. 4C, a second barrier layer 46 is formed over the first barrier layer 45. The second barrier layer 46 can be, for example, a titanium/titanium nitride (Ti/TiN) composite layer, a tungsten nitride (WN) layer , a tantalum (Ta) layer or a tantalum nitride (TaN) layer formed using a chemical vapor depositon method.

Finally, as shown in Fig. 4D, conductive material such as tungsten, copper or aluminum is deposited over the dielectric layer 42 and fills the first opening 44 and the second opening 43. Then, the conductive layer is polished to expose the dielectric

layer 42 using a chemical-mechanical polishing method. Hence, a via structure formed by a damascene process is established. The advantage of using a damascene process includes its capacity for forming both a via and a second metallic line structrue in the same processing operation. For example, a via structure is formed in the second opening 43, while a second metallic line structure is formed in the first opening 44.

As a summary, the method of forming a barrier layer includes the following characteristics:

(1) The first barrier layer 34, for example, a doped silicon (doped-Si) layer, is able to increase its adhesion with the organic low-k dielectric layer 32.

(2) The first barrier layer 34 is able to protect the surface of the organic low-k dielectric layer 32. Hence, the effect of having moisture in the dielectric layer 32 will be minimized.

(3) The first barrier layer 34 of this invention is able to reduce stress between the dielectric layer 32 and subsequently deposited metallic layer 36.

(4) The first barrier layer 34 together with the second barrier layer 35 increase the capacity to seal off diffusion of subsequently deposited metallic layer 36.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A barrier layer structure comprising:

a semiconductor substrate having a conductive layer formed thereon;

a dielectric layer over the conductive layer and the semiconductor substrate, the dielectric layer having an opening to expose the conductive layer;

a silicon-containing first barrier layer over the sides of the opening and surrounding area; and

a second barrier layer over the first barrier layer.

2. The structure of claim 1, wherein the conductive layer includes the source/drain region of a transistor.

3. The structure of claim 1, wherein the conductive layer includes a metal line structure.

4. The structure of claim 1, wherein the dielectric layer includes an organic low-k dielectric layer.

5. The structure of claim 1, wherein the first barrier layer includes a doped silicon (doped-Si) layer.

6. The structure of claim 1, wherein the first barrier layer has a thickness below 300Å.

7. The structure of claim 1, wherein the second barrier layer includes a titanium/titanium nitride (Ti/TiN) composite layer.

8. The structure of claim 1, wherein the second barrier layer includes a tungsten nitride (WN) layer.

9. The structure of claim 1, wherein the second barrier layer includes an tantalum (Ta) layer.

10. The structure of claim 1. wherein the second barrier layer includes a tantalum nitride (TaN) layer.

11. A method of forming a barrier layer comprising the steps of :

providing a semiconductor substrate that has a conductive layer formed thereon;

forming a dielectric layer over the conductive layer and the semiconductor substrate and then forming an opening in the dielectric layer to expose the conductive layer;

forming a silicon-containing first barrier layer over the sides of the opening and surrounding area; and

forming a second barrier layer over the first barrier layer.

12. The method of claim 11. wherein the conductive layer includes the source/drain region of a transistor.

13. The method of claim 11. wherein the conductive layer includes a metal line structure.

14. The method of claim 11. wherein the step of forming the dielectric layer includes depositing an organic. low-k dielectric.

15. The method of claim 11. wherein the step of forming the first barrier layer includes depositing doped silicon (doped-Si).

16. The method of claim 11. wherein the first barrier layer has a thickness below 300Å.

17. The method of claim 11. wherein the step of forming the first barrier layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

18. The method of claim 11. wherein the step of forming the first barrier layer

includes a low-pressure chemical vapor deposition (LPCVD) method.

19. The method of claim 11, wherein the step of forming the first barrier layer includes an electron beam evaporation method.

20. The method of claim 11, wherein the step of forming the first barrier layer includes a sputtering method .

21. The method of claim 11, wherein the step of forming the second barrier layer includes depositing titanium (Ti) and then titanium nitride (TiN) to form a titanium/titanium nitride (Ti/TiN) composite layer.

22. The method of claim 11, wherein the step of forming the second barrier layer includes depositing tungsten nitride (WN).

23. The method of claim 11, wherein the step of forming the second barrier layer includes depositing tantalum (Ta).

24. The method of claim 11, wherein the step of forming the second barrier layer includes depositing tantalum nitride (TaN).

25. The method of claim 11, wherein after the step of forming the second barrier layer over the first barrier layer further includes depositing a conductive material into the opening followed by a chemical-mechanical polishing (CMP) operation.

26. The method of claim 25, wherein the material used for forming the conductive layer is selected from a group that includes tungsten, copper and aluminum.

27. A method for forming a barrier layer that can be applied to a damascene process, comprising the steps of :

providing a semiconductor substrate that has a conductive layer formed thereon;

forming a dielectric layer over the conductive layer and the semiconductor

substrate and then forming a first opening in the dielectric layer, wherein the depth of the first opening is smaller than the thickness of the dielectric layer;

forming a second opening that exposes the conductive layer by continuing to etch down from the first opening, wherein the width of the second opening is smaller than the first opening;

forming a silicon-containing first barrier layer over the sides of the first opening, the second opening and surrounding area; and

forming a second barrier layer over the first barrier layer.

28. The method of claim 27, wherein the step of forming the dielectric layer includes depositing an organic low-k dielectric.

29. The method of claim 27, wherein the step of forming the first barrier layer includes depositing doped silicon (doped-Si).

30. The method of claim 27, wherein the first barrier layer has a thickness below 300Å.

31. The method of claim 27, wherein the step of forming the first barrier layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

32. The method of claim 27, wherein the step of forming the first barrier layer includes a low-pressure chemical vapor deposition (LPCVD) method.

33. The method of claim 27, wherein the step of forming the first barrier layer includes an electron beam evaporation method.

34. The method of claim 27, wherein the step of forming the first barrier layer includes a sputtering method.

35. The method of claim 27, wherein the material forming the second barrier layer is selected from a first group that includes titanium/titanium nitride (Ti/TiN), tungsten

nitride (WN), tantalum (Ta) and tantalum nitride (TaN).

36. The method of claim 27, wherein after the step of forming the second barrier layer over the first barrier layer, further includes depositing a conductive material into the first opening and the second opening followed by a chemical-mechanical polishing (CMP) operation.

37. The method of claim 36, wherein the material of forming the conductive layer is selected from a second group that includes tungsten, copper and aluminum.

38. A barrier layer structure substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3A to 4D of the accompanying drawings.

39. A method for forming a barrier layer, substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3A to 4D of the accompanying drawings.

The Patent Office

15

INVESTOR IN PEOPLE

Application No:	GB 9819997.9	**Examiner:**	Martyn Dixon
Claims searched:	all	**Date of search:**	7 January 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K (KHAAB,KHAAX,KHABP,KHABX,KHAX)

Int Cl (Ed.6): H01L (21/285,21/3205,21/786,23/532)

Other: Online: EPODOC,WPI,JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2314456 A	(Hyundai) see especially page 5, lines 16-21	1,2,5,11, 12,15
X	EP 0488576 A	(AT&T) see fig 2	1,2,5-12, 15,16, 21-26
X	EP 0315422 A	(Fujitsu) see especially col 7, lines 18-21	1,2,5,11, 12,15
X	EP 0305296 A	(Fujitsu) see layers 13,14	1,2,6,11, 12,16,20
X	US 5686323 A	(Canon) see e.g. col 5, lines 5-12	1,2,11, 12,20
A	US 5604156 A	(Samsung)	27

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.